**# Title:**

Code First – Errata: Arm CPER Processor Error Type values defined incorrectly

**# Status:**

Draft

**# Document:**

UEFI Specification 2.11 (Future Errata)

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**# Summary of the change**

**Problem Statement:**

The bit definitions for the Type field in ARM Processor Error Information Structure were newly added and published in the UEFI Specifications version 2.9A.

See N.2.4.4.1 ARM Processor Error Information, Table N-17 ARM Processor Error Information Structure, UEFI specification version 2.10 ([14. Common Platform Error Record (CPER) — UEFI Specification 2.10 documentation](https://uefi.org/specs/UEFI/2.10/Apx_N_Common_Platform_Error_Record.html#arm-processor-error-information-structure))

However, these values were defined incorrectly against the conventions. This ECR intends to correct these values.

Proposal:

There is a patch on the edk2 mailing list that adds the CPER definitions for ARM at <https://edk2.groups.io/g/devel/message/86558> The patch is currently defining the Type field bits as below

Bit 0: Cache Error

Bit 1: TLB Error

Bit 2: Bus Error

Bit 3: Vendor Error

Linux seems to be already doing this as well:

<https://elixir.bootlin.com/linux/latest/source/include/linux/cper.h#L273>

However, UEFI specification wrongly defines them as

Bit 1 - Cache Error

Bit 2 - TLB Error

Bit 3 - Bus Error

Bit 4 - Micro-architectural Error

All other values are reserved

**# Benefits of the change**

We need to update the UEFI spec to correct these values to be consistent with FW/OS implementations.

**# Impact of the change**

* **Platform FW:**
  + Use the defined values, per the EDK submitted patch
* **Operating Systems:**
  + Use the defined values. Linux already doing this.
* **Compliance tests**
  + None

**# Detailed description of the change [normative updates]**

* Insertions highlighted
* Removals in ~~red~~

N.2.4.4.1 ARM Processor Error Information

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**Table N-17 ARM Processor Error Information Structure**

|  |  |  |  |
| --- | --- | --- | --- |
| **Mnemonic** | **Byte Offset** | **Byte Length** | **Description** |
| Version | 0 | 1 | 0  (revision of this table) |
| Length | 1 | 1 | 32  (length in bytes) |
| Validation Bit | 2 | 2 | The validation bit mask indicates whether or not each of the following fields is valid in this section.  Bit 0 – Multiple Error (Error Count) Valid  Bit 1 – Flags Valid  Bit 2 – Error Information Valid  Bit 3 – Virtual Fault Address  Bit 4 – Physical Fault Address  All other bits are reserved and must be zero. |
| Type | 4 | 1 | ~~Bit 1 - Cache Error~~  ~~Bit 2 - TLB Error~~  ~~Bit 3 - Bus Error~~  ~~Bit 4 - Micro-architectural Error~~  ~~All other values are reserved~~  Bit 0 - Cache Error  Bit 1 - TLB Error  Bit 2 - Bus Error  Bit 3 - Micro-architectural Error  All other values are reserved |
| … | … | … | … |